

DSP Tools, Inc.

SDR-4000, an FPGA-Based board for RF Digital Signal Processing

Introduction

Designed for Software Defined Radio, Signal Intelligence, Radar and Test and Measurement applications, the SDR-4000 board combines an RF Front End, High Performance ADC, a 4 million gate Xilinx FPGA and a very fast USB 2.0 interface to provide a small but powerful RF processing board. PC interface software is available to stream data into a PC application, to a file or directly to MATLAB. Applications for this product include:

- Software Defined Radio
- Signal Intelligence
- Radio or Radar Signal Characterization
- Signal Acquisition for MATLAB analysis and visualization
- Multiple Channel Demodulation
- Rebroadcast Systems
- Direction Finding
- Transmitter Location

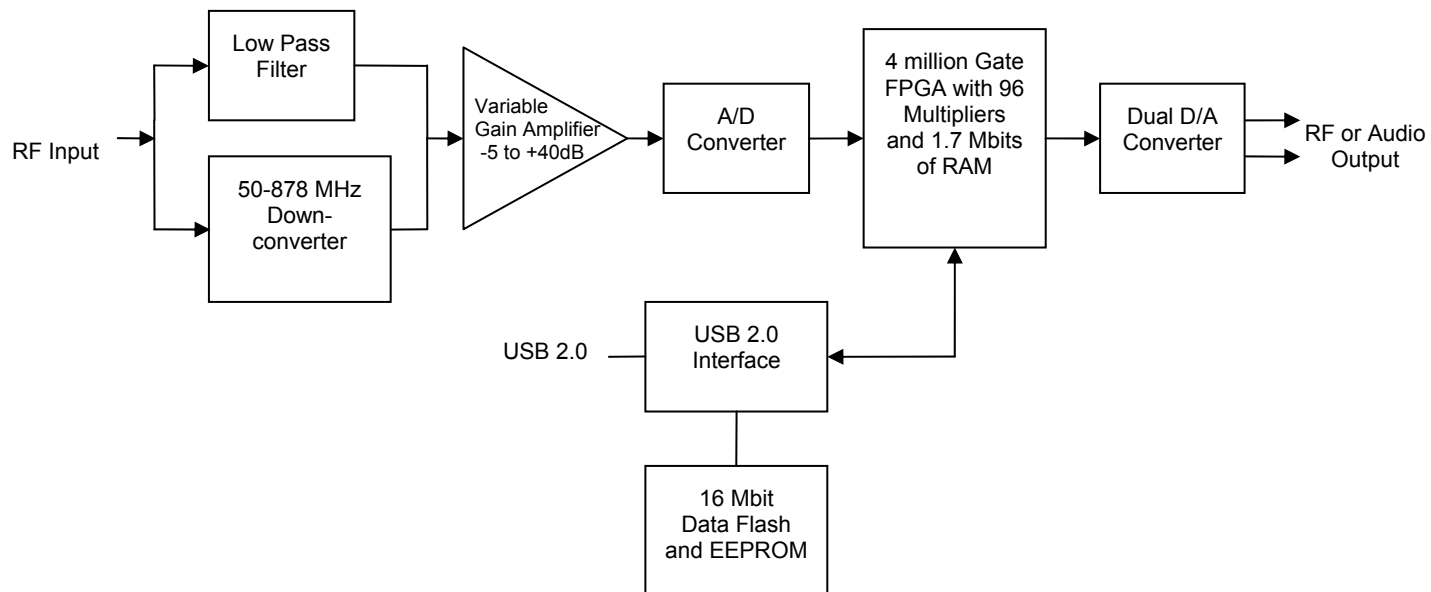
The SDR-4000 includes RF front end circuitry that allows the processing of RF signals from nearly DC to about 900 MHz. The RF front end provides adjustable gain and RF down conversion. The RF front end feeds one of the fastest 14-bit Analog to Digital Converters available. Following the ADC, a 4 million gate Xilinx FPGA with 96 multipliers and 1.7 M bits of block RAM provides a powerful, reconfigurable signal processing capability.

A 480 megabit per second USB 2.0 interface with fast FIFO-based data pipes is used to stream data between the FPGA and the computer. The FPGA configuration is downloaded from a file on the computer in less than one second, providing rapid FPGA reconfiguration that can completely change the board's algorithms. Unlike many FPGA boards, the SDR-4000 connects directly to a computer's USB port and requires only +5 volts. So a complete signal processing system doesn't need a VME rack or a PCI slot.

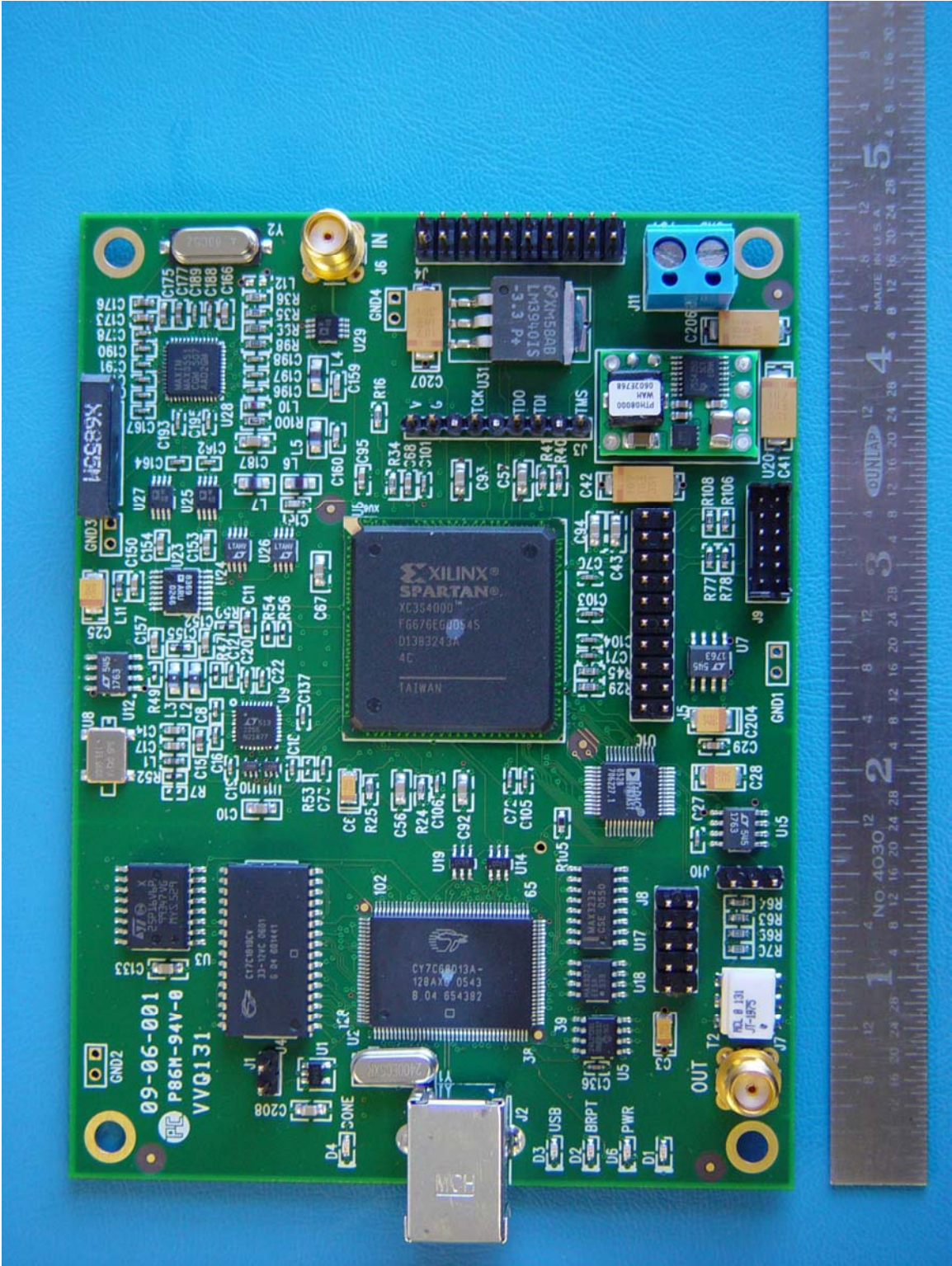
The major features of the SDR-4000 are highlighted below:

- RF Front End on board includes a Variable Gain Amplifier to increase the ADC's dynamic range
- RF Down Converter extends board's useful range from nearly DC to about 900 MHz
- 14-bit, 125 MHz ADC

- Xilinx FPGA with 4 million gates, 96 multipliers and 1.7 M bits of RAM
- JTAG port for FPGA debugging
- 480 M bit/sec USB 2.0 interface
- 4 separate FIFO-based data streams to/from computer
- Rapid FPGA configuration from a PC file via the USB interface
- MATLAB interface software and examples included
- 32 FPGA I/O pins available on connectors for general use
- FPGA I/O signals allow several boards to be interconnected and synchronized for multi-input applications such as DF and Beam Forming
- 2 Fast DAC outputs for RF, audio or two channel (I/Q) outputs
- Physically small 3.5 by 4.75 inches
- Uses a single +5 volt power supply
- May be used as a stand alone signal processor without a computer



SDR-4000 Block Diagram
Figure 1



General Description

Figure 1 shows a simplified block diagram of the SDR-4000. The board's RF input SMA connector feeds an RF front end containing two signal paths to the ADC. A signal from the FPGA called "Lowband" controls RF switch ICs to route the RF. When the "Lowband" signal is true, the input signal passes through a low pass anti-aliasing filter and then to the input of a Variable Gain Amplifier. The VGA is digitally controlled by 4 bits from the FPGA and provides a gain range of -5 to + 40 dB in 3 dB steps. Many applications, such as the Software Defined Radio receiver described below, use the VGA to implement an Automatic Gain Control to extend the ADC's dynamic range. In the Software Defined Radio application, the GUI provides a listbox allowing the user to select one of the 16 available gains, or "Automatic." In the Automatic position, circuitry in the FPGA tracks the peaks of the ADC output and adjusts the VGA control to keep the peaks near the circuit's set point.

When "Lowband" is low, the RF Input is fed to a cable television tuner IC which down converts any 6 MHz portion of the 50 MHz to 878 MHz frequency range to a center frequency of 44 MHz. That signal passes through the VGA to the ADC.

The board uses a 14-bit 125 MHz ADC converter (Linear Technologies LTC2255). A low jitter crystal oscillator provides the sample rate to the ADC and to the FPGA. Other sampling frequencies can be provided. Contact the factory for availability. The SDR-4000 was designed so that several of the boards can be interconnected for multi-input applications such as Direction Finding (DF) and Beam Forming. In multi-board applications, the FPGA's I/O signals, which may be configured to be LVDS, are used to share a sampling clock and trigger signals. In that case, several boards run synchronously. Each FPGA contains a large amount of block RAM, so synchronized multi-channel signal snapshot capture is easily done.

The ADC output flows into a Xilinx Spartan 3 (XC3S4000-4FG676C), which contains 4 million programmable gates, 96 multipliers and 1.7 mega-bits of block RAM. This is a huge amount of logic in which to implement signal processing algorithms. As an example, the Rebroadcast application that DSP Tools designed for one of our clients implemented four digital down converters each with adjustable bandwidth and FIR filters, AGC at baseband, AM, FM and single sideband demodulation, four digital up converters and FIFO buffers, allowing three independently flow controlled streams of data to the computer. All that took only 53% of the FPGA.

The SDR-4000 also contains two high-speed Digital to Analog converters that may be used for RF outputs, audio or as two test ports to view internal FPGA values while debugging an FPGA design.

The SDR-4000 uses the Cypress EZ-USB FX2 LP for its USB 2.0 interface. The Cypress part's firmware is automatically downloaded over the USB each time the board is connected. This allows changes to be made to all of the board's software and to the circuitry implemented in the FPGA just by changing the downloaded files on the computer, making it truly "Software Defined."

The EZ-USB interface processor does not get in the way of high-speed data transfers. The processor sets up the data streams and then "gets out of the way," letting FIFOs implemented in the FPGA to handle all data streaming and flow control.

Two Application Examples

To illustrate the features of the SDR-4000, two applications designed for the board are presented in the next two sections.

The two application examples are a Software Defined Radio and a Rebroadcast System. The Software Defined Radio application was designed first, and during that design many useful blocks were developed that were re-used in the Rebroadcast System design. The re-use allowed the second application to be completed in about one month. It is likely that future designs for the SDR-4000 will be rapidly developed and fielded by building on the growing assortment of tested functional blocks.

Software Defined Radio Application Example

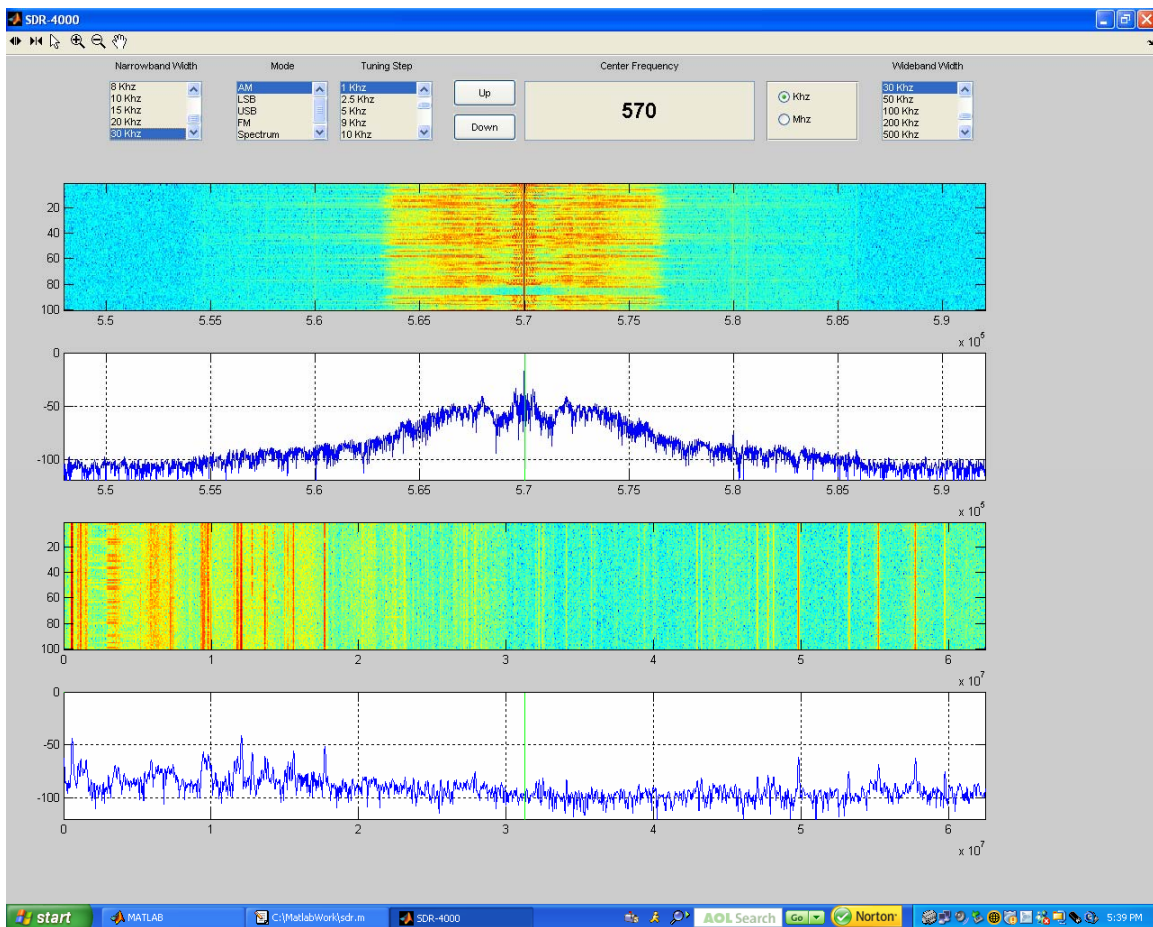
The figure on the next page shows the Windows™-based operator interface, which provides a spectrum display and a falling raster for two different portions of the frequency spectrum. To accomplish this, the FPGA contains two Digital Down Converters (DDC), each with its own bandwidth and center frequency controls. In the radio modes of operation, namely AM, Lower and Upper single sideband and FM, both DDCs are tuned to the same frequency, with one set for narrow bandwidth and the other a wider bandwidth. The In-phase and Quadrature components of each DDC output stream through separate End Points to the PC. The falling raster display is a plot in which time is displayed vertically, frequency is horizontal and the color indicates signal strength. As new spectral data is added to the display, the old data is scrolled down so it provides a history of the spectrum.

The display of the narrow band DDC shows the area immediately around the current station. A hand tool is provided on the user interface and may be used to drag the spectrum for fine frequency tuning. That tool may also be used in the wideband display to quickly tune over a large portion of the band. The bandwidth can be user selected up to 6 MHz wide. This is the bandwidth of the downconverter that is centered at the current tuned frequency.

A spectrum scan mode is provided in which audio is not produced. In this mode there are no restrictions on the center frequencies or bandwidths of the two frequency displays. They may span the entire receiver's range, from nearly DC to almost 900 MHz.

The operator can click on a signal in either of the spectrum displays to tune to a signal. Windows list boxes are used to allow the user to select the receiver bandwidths, demodulation type and tuning step. The receiver frequency can be entered in either MHz or KHz, and buttons are provided to tune up or down one tuning step at a time.

Another feature is the ability to record either a signal's demodulator output, the complex components of either DDC's output or the spectrum to a file on the computer. Signal snapshots and continuous data streams can also be passed to MATLAB™ based signal analysis tools.



Rebroadcast System Application Example

A Rebroadcast System is used in tunnels and large buildings to provide radio coverage in an area where radio signals would not usually penetrate. For example, as you drive through a tunnel under a harbor or river, your car radio continues to receive the station you were listening to before you entered the tunnel, even though you are hundreds of feet below the water's surface inside a concrete tube reinforced with a grid of steel rods. In an emergency, your radio station would be replaced by announcements from the tunnel authority or an emergency team. A Rebroadcast System is used to provide this capability.

A typical rebroadcast system has an outside antenna and tuners for 16 AM and 16 FM stations. The tuners receive each station, down converting and bandpass filtering each. The signals are mixed down to baseband, each one is AGC'ed and then mixed back up to each station's original frequency. Emergency announcements may replace the received stations, allowing communication to each car via their car radio receivers. In the past, a rebroadcast system for 32 stations used individual radios for each channel and occupied two 6 foot high racks of circuitry.

DSP Tools, Inc. used SDR-4000 boards to replace all that circuitry by digitally processing 4 channels on each small board. After conversion to digital form by the ADC on the SDR-4000 board, all processing was done digitally in the board's FPGA. Each channel implemented a Digital Down Converter for tuning, mixing to baseband and bandpass filtering each station. The baseband signals were digitally AGC'ed and then Digital Up Converted in the FPGA to their original station frequency. Each Digital Up Converter contained an interpolator to increase the complex digital baseband signal sample rate to 125 mega-samples per second. Each channel's Direct Digital Synthesizer produced digital Sine and Cosine carrier frequency signals to mix the interpolator outputs up to the original station frequencies. The four channels in each FPGA were summed digitally and fed to the board's high-speed DAC for conversion back to an analog RF output. As a test feature, a demodulator was added to the FPGA design to allow the monitoring of each received station. The four channels occupied only about half of the FPGA, so it is likely that 8 channels would fit, since there is a good amount of logic that is common to all channels. However, the size and cost reduction was so dramatic that our client chose to do only 4 channels per board, leaving the remaining room for future features.

Custom Application Design and Consulting

The engineers at DSP Tools can provide design assistance for any portion or all of your design, including FPGA design, device interface software, signal analysis, computer applications and data visualization. We invite you to call us to talk about your project.